

1 What is claimed is:

2 1. A method of forming a portion of a semiconductor integrated circuit;

3 comprising the steps of:

4 growing a field oxide across the integrated circuit;

5 patterning and etching the field oxide to form an opening with substantially
6 vertical sidewalls exposing a portion of an upper surface of a substrate underlying the
7 field oxide where an active area will be formed;

8 growing a gate oxide over the exposed portion of the substrate;

9 depositing a polysilicon layer over the field oxide and gate oxide to a thickness
10 wherein the lowest most portion of the upper surface of the polysilicon is above the
11 upper surface of the field oxide;

12 planarizing the polysilicon layer;

13 forming a photoresist mask over a portion of the polysilicon layer overlying at
14 least a portion of the substrate not covered by the field oxide;

15 patterning and etching the polysilicon and gate oxide to form a gate electrode;

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1 removing the photoresist; and

2 forming sidewall spacers along the sides of the gate electrode.

3 2. The method of claim 1, wherein the field oxide has a thickness of between
4 approximately 4000-5000 angstroms.

5 3. The method of claim 1, further comprising the steps of:

6 forming an n-well in the substrate before the field oxide is formed in areas where
7 the field oxide will be removed.

8 4. The method of claim 3, wherein the n-well is formed by implantation and
9 drive-in of phosphorous.

10 5. The method of claim 1, further comprising the step of:

11 performing a blanket implant in the substrate to adjust to desired doping levels
12 before forming the gate oxide layer.

13 6. The method of claim 5, wherein the blanket implant comprises boron
14 implanted at a dosage of approximately $1.5 \times 10^{12}/\text{cm}^2$ at 30 KeV.

1 11. The method of claim 1, further comprising the steps of:

2 masking off selected n-well regions in the substrate; and

3 implanting a dopant into the p-type regions to adjust to a desired doping level.

4 12. The method of claim 11, wherein the dopant comprises boron implanted at a
5 dosage of approximately $6 \times 10^{12}/\text{cm}^2$ and at approximately 180 KeV.

6 13. The method of claim 1, wherein the gate oxide has thickness of between
7 approximately 70-100 angstroms.

8 14. The method of claim 1, wherein the polysilicon layer is formed to a thickness
9 of between approximately 7000-9000 angstroms.

10 15. The method of claim 1, wherein the polysilicon is in-situ doped as deposited.

11 16. The method of claim 1, further comprising the step of:

12 doping the polysilicon to a desired doping level after deposition.

1 17. The method of claim 1, wherein the step of planarizing the polysilicon
2 comprises CMP.

3 18. The method of claim 1, wherein the step of planarizing the polysilicon
4 comprises the steps of:

5 forming a planar layer over the polysilicon layer having an etch ratio of 1:1 with
6 the polysilicon;

7 performing an etchback of the planar layer and polysilicon.

8 19. The method of claim 18, wherein the planar layer is spin-on-glass.

9 20. The method of claim 18, wherein the planar layer is photoresist.

10 21. The method of claim 18, wherein the etchback comprises a wet etch.

11 22. The method of claim 18, wherein the etchback comprises chemical
12 mechanical polishing.

13 23. The method of claim 18, wherein there remains a layer of polysilicon above
14 the surface of the field oxide and in the opening after the polysilicon is etched.

1 29. The method of claim 28, wherein the silicide is formed from the group
2 consisting of tantalum, tungsten, titanium and molybdenum.

3 30. The method of claim 28, wherein the silicide has a thickness of between
4 approximately 1200-1700 angstroms.

5 31. The method of claim 1, further comprising the step of:

6 forming a capping layer over the polysilicon layer before the photoresist is
7 formed; and

8 etching the silicide along with the polysilicon.

9 32. The method of claim 31, wherein the capping layer comprises oxide.

10 33. The method of claim 31, wherein the capping oxide has a thickness of
11 between approximately 1200-1700 angstroms.

12 34. The method of claim 1, further comprising the step of:

13 forming lightly doped drain regions in the substrate adjacent the gate electrode
14 before the sidewall spacers are formed.

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1 37. The method of claim 36, wherein the step of forming a raised source/drain
2 further comprises the steps of:

3 forming a capping layer over the polysilicon layer before the photoresist is
4 formed;

5 etching the capping layer with the polysilicon layer;

6 depositing a polysilicon layer over the transistor gate electrode, exposed
7 substrate and the field oxide wherein the lowest most portion of the upper surface of the
8 polysilicon layer is above the upper surface of the gate electrode;

9 forming a planar sacrificial layer over the polysilicon layer having a 1:1 etch rate
10 with the polysilicon layer;

11 etching the sacrificial layer and the polysilicon layers exposing the upper surface
12 of the field oxide;

13 doping the polysilicon layer to a desired doping level.

14 38. The method of claim 37, wherein the lowest most portion of the upper
15 surface of the polysilicon layer is above the upper surface of the gate electrode.

1 39. The method of claim 37, further comprising the step of:
2 forming a silicide under the capping layer and over the polysilicon before the
3 polysilicon is deposited.

4 40. The method of claim 36, wherein the step of forming a raised source/drain
5 further comprises the steps of:

6 selectively growing epitaxy above the exposed substrate surface;

7 implanting the epitaxy with an appropriate dopant to achieve a desired
8 conductivity level; and

9 siliciding an upper portion of the selectively grown epitaxy.
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1 41. A method of forming a portion of a semiconductor integrated circuit;
2 comprising the steps of:

3 growing a field oxide across the integrated circuit;

4 patterning and etching the field oxide to form an opening with substantially
5 vertical sidewalls exposing a portion of an upper surface of a substrate underlying the
6 field oxide where an active area will be formed;

7 growing a gate oxide over the exposed portion of the substrate;

8 depositing a doped polysilicon layer over the field oxide and gate oxide to a
9 thickness wherein the lowest most portion of the upper surface of the polysilicon is
10 above the upper surface of the field oxide;

11 planarizing and etching the polysilicon layer such that the upper surface of the
12 polysilicon layer remains at or above the upper surface of the field oxide;

13 forming a silicide over the polysilicon layer;

14 forming a capping layer over the silicide;

1 50. The structure of claim 48, further comprising:

2 an n-well in the active area in the substrate.

3 51. The structure of claim 48, wherein the gate oxide has a thickness of
4 between approximately 70-100 angstroms.

5 52. The structure of claim 48, wherein the polysilicon gate electrode has a
6 thickness of between approximately 7000-9000 angstroms.

7 53. The structure of claim 48, further comprising:

8 a silicide layer over the polysilicon gate electrode.

9 54. The structure of claim 53, wherein the silicide is from the group consisting of
10 tantalum, tungsten, titanium and molybdenum.

11 55. The method of claim 53, wherein the silicide has a thickness of between
12 approximately 1200-1700 angstroms.

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1 48. A structure consisting of a portion of a semiconductor integrated circuit,
2 comprising:

3 a field oxide formed across the integrated circuit having an opening therethrough
4 with substantially vertical sidewalls exposing a portion of an upper surface of a
5 substrate underlying the field oxide;

6 a gate oxide over a portion of the exposed portion of the substrate;

7 a polysilicon gate electrode overlying the gate oxide and having an upper
8 surface planar with or above an upper surface of the field oxide;

9 LDD regions in the substrate adjacent the gate electrode; and

10 sidewall spacers along the sides of the polysilicon gate electrode.

11 49. The structure of claim 48, wherein the field oxide has a thickness of between
12 approximately 4000-5000 angstroms.

- 1 56. The structure of claim 48, further comprising:
- 2 a capping layer over the silicide.
- 3 57. The structure of claim 56, wherein the capping layer comprises oxide.
- 4 58. The structure of claim 56, wherein the capping layer has a thickness of
- 5 between approximately 1200-1700 angstroms.
- 6 59. The structure of claim 48, further comprising:
- 7 LDD regions in the substrate adjacent the gate electrode.
- 8 60. The structure of claim 48, further comprising:
- 9 source/drain regions adjacent the gate electrode in the substrate.
- 10 61. The structure of claim 48, further comprising:
- 11 raised source/drain regions adjacent the gate electrode and overlying the
- 12 exposed substrate.

1 64. A structure consisting of a portion of a semiconductor integrated circuit,
2 comprising:

3 a field oxide formed across the integrated circuit having an opening therethrough
4 with substantially vertical sidewalls exposing an active area in a portion of an upper
5 surface of a substrate underlying the field oxide;

6 a gate oxide over a portion of the exposed substrate;

7 a polysilicon gate electrode overlying the gate oxide and having an upper
8 surface planar with or above the upper surface of the field oxide;

9 a silicide layer over the polysilicon layer;

10 a capping layer over the silicide layer;

11 LDD regions in the substrate adjacent the gate electrode; and

12 sidewall spacers along the sides of the polysilicon gate electrode.
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